CLAIM AMENDMENTS

1-14 (Cancelled)

15. (Currently Amended) A method of making a flip chip assembly, comprising:

attaching a substrate to a semiconductor chip, wherein the substrate includes a dielectric layer and metallization, the dielectric layer includes first and second surfaces that are opposite one another and a via hole that extends between the first and second surfaces, the metallization is disposed on walls of the via hole and extends along the walls to the first and second surfaces, the chip includes a terminal pad that is aligned with the via hole, and a reflowable material that contains solder contacts the metallization and the pad; and then

reflowing the reflowable material to provide an electrical connection between the metallization and the pad.

16. (Previously Presented) The method as recited in claim 15, wherein the reflowable material is deposited on the metallization before attaching the substrate to the chip, and during the reflowing the reflowable material wets and flows on an exposed portion of the pad beneath the via hole.

17. (Withdrawn) The method as recited in claim 15, wherein the reflowable material is deposited on the pad before attaching the substrate to the chip, and during the reflowing the reflowable material wets and flows on an exposed portion of the metallization in the via hole.

18. (Previously Presented) The method as recited in claim 15, wherein the pad is directly beneath substantially all surface area defined by the via hole after the attaching.

19. (Previously Presented) The method as recited in claim 15, wherein the metallization is electrolessly plated on the walls of the via hole.

20. (Previously Presented) The method as recited in claim 15, wherein the reflowable material fills a bottom portion of the via hole without filling a top portion of the via hole after the reflowing.

21. (Withdrawn) The method as recited in claim 15, wherein the reflowable material is solder paste.

22. (Previously Presented) The method as recited in claim 15, wherein the substrate remains at a fixed position relative to the chip during the reflowing.

23. (Previously Presented) The method as recited in claim 15, wherein substantially all of the reflowable material is within the via hole after the reflowing.

24. (Previously Presented) The method as recited in claim 15, wherein the metallization and the reflowable material are the only materials in the via hole after the reflowing.

25. (Currently Amended) A method of making a flip chip assembly, comprising the following steps in the sequence set forth:

providing a substrate that includes a dielectric layer, wherein the dielectric layer includes first and second surfaces that are opposite one another and a via hole that extends between the first and second surfaces;

depositing metallization on walls of the via hole such that the metallization extends along the walls to the first and second surfaces;

depositing solder on the metallization such that the solder is disposed in the via hole;

attaching the substrate to a semiconductor chip that includes a terminal pad, wherein the first surface faces away from the chip, the second surface faces towards the chip, the via hole is aligned with the pad and the solder contacts the pad; and

applying heat to reflow the solder to form a solder joint that contacts and electrically connects the metallization and the pad and prevents the via hole from exposing the pad.

26. (Previously Presented) The method as recited in claim 25, including depositing the metallization on the walls using electroless plating.

27. (Previously Presented) The method as recited in claim 25, including depositing the metallization on the walls such that substantially all of the metallization is within the via hole.

28. (Currently Amended) The method as recited in claim 25, including depositing the metallization on the walls such that the metallization provides a plated through-hole~~extends along the walls to the first and second surfaces~~.

29. (Previously Presented) The method as recited in claim 25, including depositing the metallization on the walls such that the metallization is aligned with the second surface.

30. (Previously Presented) The method as recited in claim 25, including depositing the solder on the metallization using electroplating.

31. (Withdrawn) The method as recited in claim 25, including depositing the solder on the metallization using electroless plating.

32. (Withdrawn) The method as recited in claim 25, including depositing the solder on the metallization using wave soldering.

33. (Withdrawn) The method as recited in claim 25, including depositing the solder on the metallization using meniscus coating.

34. (Withdrawn) The method as recited in claim 25, including depositing the solder on the metallization using solder paste printing.

35. (Previously Presented) The method as recited in claim 25, including depositing the solder on the metallization such that solder extends along the metallization to the first and second surfaces.

36. (Previously Presented) The method as recited in claim 25, including attaching the substrate to the chip such that the via hole exposes the pad.

37. (Previously Presented) The method as recited in claim 25, including attaching the substrate to the chip such that the pad is directly beneath substantially all surface area defined by the via hole.

38. (Previously Presented) The method as recited in claim 25, including attaching the substrate to the chip using an adhesive between the substrate and the chip.

39. (Withdrawn) The method as recited in claim 25, including attaching the substrate to the chip using a mechanical clamp.

40. (Previously Presented) The method as recited in claim 25, including applying the heat to reflow the solder using a convection oven.

41. (Withdrawn) The method as recited in claim 25, including applying the heat to reflow the solder using a laser.

42. (Withdrawn) The method as recited in claim 25, including applying the heat to reflow the solder using an infrared continuous belt reflow oven.

43. (Withdrawn) The method as recited in claim 25, including applying the heat to reflow the solder using hot nitrogen gas.

44. (Withdrawn) The method as recited in claim 25, including applying the heat to reflow the solder using a vapor phase reflow system.

45. (Previously Presented) The method as recited in claim 25, including applying the heat to reflow the solder such that substantially all of the solder joint is within the via hole.

46. (Previously Presented) The method as recited in claim 25, including applying the heat to reflow the solder such that the solder joint fills a bottom portion of the via hole without filling a top portion of the via hole.

47. (Previously Presented) The method as recited in claim 25, including applying the heat to reflow the solder such that the solder wets and covers an exposed portion of the pad.

48. (Previously Presented) The method as recited in claim 25, including applying the heat to reflow the solder while maintaining the substrate at a fixed position relative to the chip.

49. (Previously Presented) The method as recited in claim 25, wherein the metallization and the solder joint are the only materials in the via hole after applying the heat.

50. (Withdrawn) A method of making a flip chip assembly, comprising the following steps in the sequence set forth:

providing a semiconductor chip that includes a terminal pad;

depositing solder on the pad;

attaching a substrate to the chip, wherein the substrate includes a dielectric layer and metallization, the dielectric layer includes first and second surfaces that are opposite one another and a via hole that extends between the first and second surfaces, the metallization is disposed on walls of the via hole and extends along the walls to the first and second surfaces, the via hole is aligned with the pad and exposes the solder, the solder contacts the metallization, the metallization is spaced from the pad, the first surface faces away from the chip, the second surface faces towards the chip, and the substrate is at a fixed position relative to the chip; and

applying heat to reflow the solder such that the solder wets and flows on the metallization in the via hole and forms a solder joint that contacts and electrically connects the metallization and the pad while the substrate remains at the fixed position relative to the chip.

51. (Withdrawn) The method as recited in claim 50, wherein the metallization is aligned with the second surface.

52. (Withdrawn) The method as recited in claim 50, wherein essentially all of the solder joint is in the via hole.

53. (Withdrawn) The method as recited in claim 50, wherein the pad is directly beneath essentially all surface area defined by the via hole after attaching the substrate to the chip.

54. (Withdrawn) The method as recited in claim 50, wherein the metallization and the solder joint are the only materials in the via hole after applying the heat.

55. (Previously Presented) A method of making a flip chip assembly, comprising the following steps in the sequence set forth:

providing a substrate that includes a dielectric layer, wherein the dielectric layer includes first and second surfaces that are opposite one another and a via hole that extends between the first and second surfaces;

electrolessly plating metallization on walls of the via hole, wherein the metallization extends along the walls to the first and second surfaces;

electroplating solder on the metallization such that the solder is disposed in the via hole;

attaching the substrate to a semiconductor chip using an adhesive therebetween, wherein the first surface faces away from the chip, the second surface faces towards the chip, the chip includes a terminal pad, the via hole is aligned with and exposes the pad, the solder contacts the pad and the metallization is spaced from the pad; and

applying heat to reflow the solder such that the solder wets and flows on the pad and forms a solder joint that contacts and electrically connects the metallization and the pad and prevents the via hole from exposing the pad.

56. (Previously Presented) The method as recited in claim 55, wherein the metallization is aligned with the second surface.

57. (Previously Presented) The method as recited in claim 55, wherein essentially all of the solder joint is in the via hole.

58. (Previously Presented) The method as recited in claim 55, wherein the pad is directly beneath essentially all surface area defined by the via hole after attaching the substrate to the chip.

59. (Previously Presented) The method as recited in claim 55, wherein the metallization and the solder joint are the only materials in the via hole after applying the heat.

60. (Previously Presented) A method of making a flip chip assembly, comprising the following steps in the sequence set forth:

providing a substrate that includes a dielectric layer and a conductive trace, wherein the dielectric layer includes first and second surfaces that are opposite one another and a via hole that extends between the first and second surfaces, and the conductive trace includes metallization disposed on walls of the via hole and a bond site disposed on the first surface and spaced from the via hole;

depositing solder on the metallization and the bond site, wherein the solder on the metallization is in the via hole, the solder on the bond site is outside the via hole, and the solder on the metallization does not contact the solder on the bond site;

attaching the substrate to a semiconductor chip, wherein the first surface faces away from the chip, the second surface faces towards the chip, the chip includes a terminal pad, the solder on the metallization contacts the pad, the metallization does not contact the pad, and the solder on the bond site does not contact the chip; and

applying heat to reflow the solder such that the solder on the metallization forms a solder joint that contacts and electrically connects the metallization and the pad, the solder on the bond site forms a solder contact that does not contact the solder joint and does not contact the chip, and the conductive trace electrically connects the solder joint and the solder contact.

61. (Previously Presented) The method as recited in claim 60, including depositing the solder on the metallization and the bond site using electroplating.

62. (Withdrawn) The method as recited in claim 60, including depositing the solder on the metallization and the bond site using electroless plating.

63. (Withdrawn) The method as recited in claim 60, including depositing the solder on the metallization and the bond site using wave soldering.

64. (Withdrawn) The method as recited in claim 60, including depositing the solder on the metallization and the bond site using meniscus coating.

65. (Withdrawn) The method as recited in claim 60, including depositing the solder on the metallization and the bond site using solder paste printing.

66. (Previously Presented) The method as recited in claim 60, wherein the metallization is aligned with the second surface.

67. (Previously Presented) The method as recited in claim 60, wherein essentially all of the solder joint is in the via hole.

68. (Previously Presented) The method as recited in claim 60, wherein the metallization and the solder joint are the only materials in the via hole after applying the heat to reflow the solder.

69. (Previously Presented) The method as recited in claim 60, wherein the pad is directly beneath essentially all surface area defined by the via hole after attaching the substrate to the chip.

70. (Previously Presented) The method as recited in claim 15, including attaching the substrate to the chip using an adhesive that does not electrically connect the substrate and the chip.

71. (Previously Presented) The method as recited in claim 15, including attaching the substrate to the chip using an adhesive that is sandwiched between and contacts the substrate and the chip and does not electrically connect the substrate and the chip.

72. (Previously Presented) The method as recited in claim 15, wherein the pad is a bumpless pad.

73. (Previously Presented) The method as recited in claim 15, wherein the pad is a solder-free pad.

74. (Previously Presented) The method as recited in claim 15, wherein the pad is a bumpless solder-free pad.

75. (Previously Presented) The method as recited in claim 25, including attaching the substrate to the chip using an adhesive that does not electrically connect the substrate and the chip.

76. (Previously Presented) The method as recited in claim 25, including attaching the substrate to the chip using an adhesive that is sandwiched between and contacts the substrate and the chip and does not electrically connect the substrate and the chip.

77. (Previously Presented) The method as recited in claim 25, wherein the pad is a bumpless pad.

78. (Previously Presented) The method as recited in claim 25, wherein the pad is a solder-free pad.

79. (Previously Presented) The method as recited in claim 25, wherein the pad is a bumpless solder-free pad.

80. (Withdrawn) The method as recited in claim 50, including attaching the substrate to the chip using an adhesive that does not electrically connect the substrate and the chip.

81. (Withdrawn) The method as recited in claim 50, including attaching the substrate to the chip using an adhesive that is sandwiched between and contacts the substrate and the chip and does not electrically connect the substrate and the chip.

82. (Withdrawn) The method as recited in claim 50, wherein the pad is a bumpless pad.

83. (Withdrawn) The method as recited in claim 50, wherein the pad is a solder-free pad.

84. (Withdrawn) The method as recited in claim 50, wherein the pad is a bumpless solder-free pad.

85. (Previously Presented) The method as recited in claim 55, including attaching the substrate to the chip using an adhesive that does not electrically connect the substrate and the chip.

86. (Previously Presented) The method as recited in claim 55, including attaching the substrate to the chip using an adhesive that is sandwiched between and contacts the substrate and the chip and does not electrically connect the substrate and the chip.

87. (Previously Presented) The method as recited in claim 55, wherein the pad is a bumpless pad.

88. (Previously Presented) The method as recited in claim 55, wherein the pad is a solder-free pad.

89. (Previously Presented) The method as recited in claim 55, wherein the pad is a bumpless solder-free pad.

90. (Previously Presented) The method as recited in claim 60, including attaching the substrate to the chip using an adhesive that does not electrically connect the substrate and the chip.

91. (Previously Presented) The method as recited in claim 60, including attaching the substrate to the chip using an adhesive that is sandwiched between and contacts the substrate and the chip and does not electrically connect the substrate and the chip.

92. (Previously Presented) The method as recited in claim 60, wherein the pad is a bumpless pad.

93. (Previously Presented) The method as recited in claim 60, wherein the pad is a solder-free pad.

94. (Previously Presented) The method as recited in claim 60, wherein the pad is a bumpless solder-free pad.

95. (Previously Presented) The method as recited in claim 15, wherein the reflowable material extends continuously between the first and second surfaces in the via hole after the reflowing.

96. (Previously Presented) The method as recited in claim 15, wherein the reflowable material is the only material in the via hole that contacts the metallization after the reflowing.

97. (Previously Presented) The method as recited in claim 15, wherein the reflowable material is the only material in the via hole that contacts the pad after the reflowing.

98. (Previously Presented) The method as recited in claim 15, wherein the reflowable material is the only material that contacts the metallization and the pad after the reflowing.

99. (Previously Presented) The method as recited in claim 15, wherein the reflowable material is the only conductor external to the chip that contacts the pad after the reflowing.

100. (Previously Presented) The method as recited in claim 25, wherein the solder joint extends continuously between the first and second surfaces in the via hole.

101. (Previously Presented) The method as recited in claim 25, wherein the solder joint is the only material in the via hole that contacts the metallization.

102. (Previously Presented) The method as recited in claim 25, wherein the solder joint is the only material in the via hole that contacts the pad.

103. (Previously Presented) The method as recited in claim 25, wherein the solder joint is the only material that contacts the metallization and the pad.

104. (Previously Presented) The method as recited in claim 25, wherein the solder joint is the only conductor external to the chip that contacts the pad.

105. (Withdrawn) The method as recited in claim 50, wherein the solder joint extends continuously between the first and second surfaces in the via hole.

106. (Withdrawn) The method as recited in claim 50, wherein the solder joint is the only material in the via hole that contacts the metallization.

107. (Withdrawn) The method as recited in claim 50, wherein the solder joint is the only material in the via hole that contacts the pad.

108. (Withdrawn) The method as recited in claim 50, wherein the solder joint is the only material that contacts the metallization and the pad.

109. (Withdrawn) The method as recited in claim 50, wherein the solder joint is the only conductor external to the chip that contacts the pad.

110. (Previously Presented) The method as recited in claim 55, wherein the solder joint extends continuously between the first and second surfaces in the via hole.

111. (Previously Presented) The method as recited in claim 55, wherein the solder joint is the only material in the via hole that contacts the metallization.

112. (Previously Presented) The method as recited in claim 55, wherein the solder joint is the only material in the via hole that contacts the pad.

113. (Previously Presented) The method as recited in claim 55, wherein the solder joint is the only material that contacts the metallization and the pad.

114. (Previously Presented) The method as recited in claim 55, wherein the solder joint is the only conductor external to the chip that contacts the pad.

115. (Previously Presented) The method as recited in claim 60, wherein the solder joint extends continuously between the first and second surfaces in the via hole.

116. (Previously Presented) The method as recited in claim 60, wherein the solder joint is the only material in the via hole that contacts the metallization.

117. (Previously Presented) The method as recited in claim 60, wherein the solder joint is the only material in the via hole that contacts the pad.

118. (Previously Presented) The method as recited in claim 60, wherein the solder joint is the only material that contacts the metallization and the pad.

119. (Previously Presented) The method as recited in claim 60, wherein the solder joint is the only conductor external to the chip that contacts the pad.